What we claim as our invention is:

1. A method for operating a pipeline in a processor comprising;

fetching a number of instructions greater than the number of execution units in a processor, and

combining a plurality of instructions into a control word which can be processed by one execution unit.

2. The method according to Claim 1 wherein:

two instructions are combined into a control word.

3. The method according to Claim 1 further comprising;

issuing the control word to an execution unit.

4. The method according to Claim 1 wherein;

said processor has four execution units and said pipeline fetches at least five instructions.

5. The method according to Claim 4 wherein;

said pipeline fetches eight instructions.

6. The method according to Claim 4 wherein;

said pipeline checks instructions for conflicts and issues valid control words to said execution units.

7. The method of Claim 6 wherein;

said pipeline issues control words to all four execution units.

8. A processor comprising:

an instruction pipeline having a first stage fetching and decoding a number of instructions greater than the number of execution units in said processor, and

fusing logic in a second stage of said pipeline combining a plurality of said decoded instructions into a control word which can be executed by one execution unit.

9. The processor of Claim 8 further including;

an issue slot in said second stage for coupling said control word to following stages of said pipeline.

10. The processor of Claim 9 further including;

an execution unit in a third stage of said pipeline receiving and executing the control word.

11. The processor of Claim 8 wherein;

said processor comprises four execution units and said first pipeline stage fetches at least five instructions.

12. The processor of Claim 11 wherein;

said pipeline fetches eight instructions.

13. The processor of Claim 8 further comprising;

grouping logic in said second stage checking said instructions for conflicts and issuing only valid control words.

14. The processor of Claim 13 wherein;

said processor comprises four issue slots receiving valid control words.

15. The processor of Claim 14 wherein;

said processor issues control words to all four execution units in one clock cycle.

16. The processor of Claim 14 wherein said processor comprises;

four execution units, each receiving control words from one of said issue slots.

17. A system for coupling instructions from memory to execution units in a processor comprising;

fetching means for fetching and decoding a number of instructions greater than the number of execution units in said processor, and

fusing means for combining a plurality of said instructions into a control word which can be executed by one execution unit.

18. The system of Claim 17 further comprising;

grouping means for checking said instructions for conflicts which would prevent simultaneous execution of said instructions.

19. The system of Claim 18 further comprising;

issue means for issuing control words which may be executed simultaneously to a plurality of said execution units.

20. The system of Claim 19 wherein;

said processor comprises four execution units and

said issue means includes slots for issuing a control word to each execution unit.

21. The system of Claim 20 wherein;

said fetching means fetches eight instructions simultaneously.